CLAIMS

1. A method for identifying faulty functional logic, comprising the operations of:

providing a normal internal clock signal for use in accessing functional logic, the functional logic having access to redundant functional logic during normal operation; and

performing a test on the functional logic using a stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration than each pulse of the normal internal clock signal, wherein functional logic elements that fail the test using the stress clock signal are identified as non-usable functional logic elements.

2. A method as recited in claim 1, wherein the non-usable functional logic elements are recorded in a memory block.

3. A method as recited in claim 2, wherein the normal internal clock signal is based on a margin added to required logic access times for functional logic elements of the functional logic, and wherein each pulse of the stress clock signal is approximately equal to each pulse of the normal internal clock signal minus the margin.

4. A method as recited in claim 1, wherein the method is performed using a generator.

5. A method for identifying faulty functional logic, comprising the operations of:

providing a normal internal clock signal for use in accessing functional logic, the functional logic having access to redundant functional logic during normal operation; and

applying a test on the functional logic using a stress clock signal, wherein each pulse of the stress clock signal is of a shorter duration than each pulse of the normal internal clock signal;

determining if logic elements of the functional logic are faulty based on the use of the stress clock signal; and

re-routing signals previously routed through the faulty logic elements through the redundant functional logic.

6. A method for identifying faulty functional logic as recited in claim 5, wherein the re-routing is performed when the faulty logic is repairable.

7. A method for identifying faulty functional logic as recited in claim 5, wherein the re-routing implements redundancy control logic and registers for storing the re-routing.

8. A method for identifying faulty functional logic as recited in claim 5, wherein the test is partially controlled through built-in self test circuitry.

9. A method for identifying faulty functional logic as recited in claim 5, wherein the faulty logic elements are recorded in a memory block.

10. A method for identifying faulty functional logic as recited in claim 5, wherein the normal internal clock signal is based on a margin added to required logic access times for functional logic elements of the functional logic, and wherein each pulse of the stress clock signal is approximately equal to each pulse of the normal internal clock signal minus the margin.

11. A method for testing a circuit, comprising:

providing a normal internal clock signal for use in accessing functional logic, the functional logic having access to redundant functional logic during normal operation; and

applying a stress clock signal to the functional logic, each pulse of the stress clock signal being of a shorter duration than each pulse of the normal internal clock signal; and

identifying logic elements of the functional logic that fail to operate as intended when operated using the stress clock signal.

12. A method for testing a circuit as recited in claim 11, further comprising:

programming a re-rout of signals previously routed through the logic elements that failed through the redundant functional logic.

13. A method for testing a circuit as recited in claim 11, wherein the normal internal clock signal is based on a margin added to required logic access times for functional logic elements of the functional logic, and wherein each pulse of the stress clock signal is approximately equal to each pulse of the normal internal clock signal minus the margin.

14. A method for testing a circuit as recited in claim 11, further comprising:

marking the failed functional logic elements as un-usable when the failed functional logic elements cannot be re-routed through the redundant functional logic.

15. A method for testing a circuit as recited in claim 11, further comprising:

recording the failed logic elements in a memory block.

16. A method for testing a circuit as recited in claim 15, wherein the memory block is defined by at least one register.

17. A method for testing a circuit as recited in claim 11, wherein the method is performed using a memory a generator.

18. A method for testing a circuit as recited in claim 11, wherein the test is partially controlled through built-in self test circuitry.